AND8431/D

Designing a Quasi-Resonant Adaptor Driven by the NCP1380

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APPLICATION NOTE

Quasi−square wave resonant converters also known as Quasi−Resonant (QR) converter are widely used in the adaptor market. They allow designing flyback Switched−Mode Power Supply (SMPS) with reduced Electro−Magnetic Interference (EMI) signature and improved efficiency. However, as the switching frequency of QR converter increases as the load decreases, the frequency must be limited.

In traditional QR converter, the frequency is limited by a frequency clamp. But, when the switching frequency of the system reaches the frequency clamp limit, valley jumping occurs: the controller hesitates between two valleys resulting in an unstable operation and noise in the transformer at medium and light output loads.

In order to overcome this problem, the NCP1380 and the NCP1379 feature a “valley lockout” circuit: the switching frequency is decreased step by step by changing valley as the load decreases. Once the controller selects a valley, it stays locked in this valley until the output power changes significantly. This technique extends the QR operation of the system towards lighter loads without degrading the efficiency.

This application note focuses on the design of an adapter driven by the NCP1380. The equations developed are further used to design a 60 W adapter. The same equations can be applied to the NCP1379.

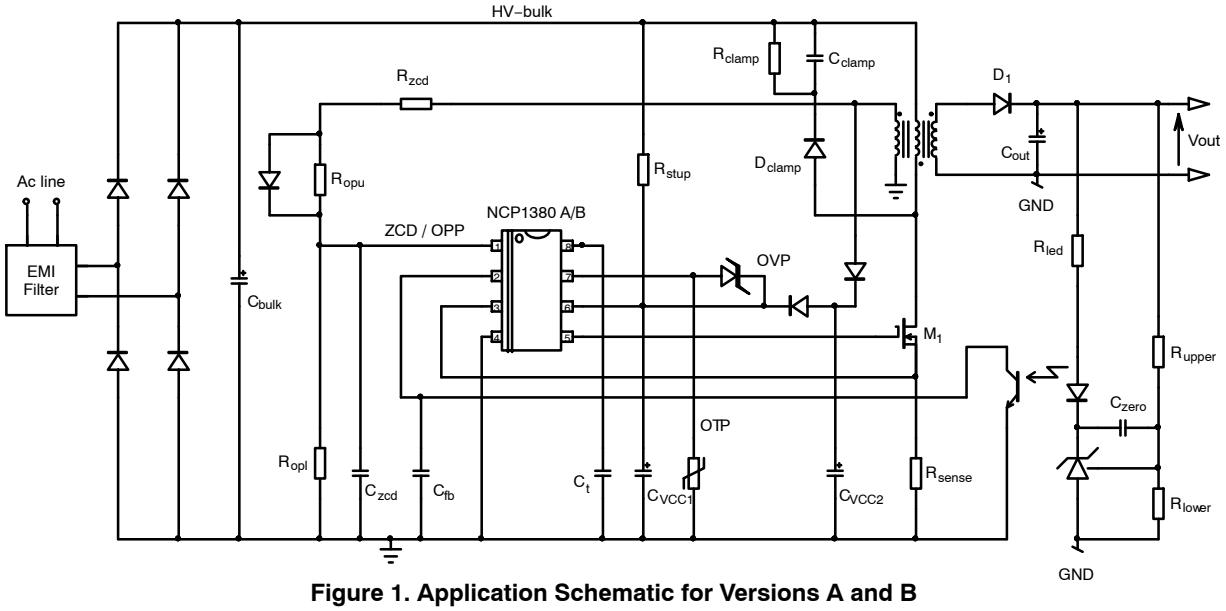

Figure 1. Application Schematic for Versions A and B

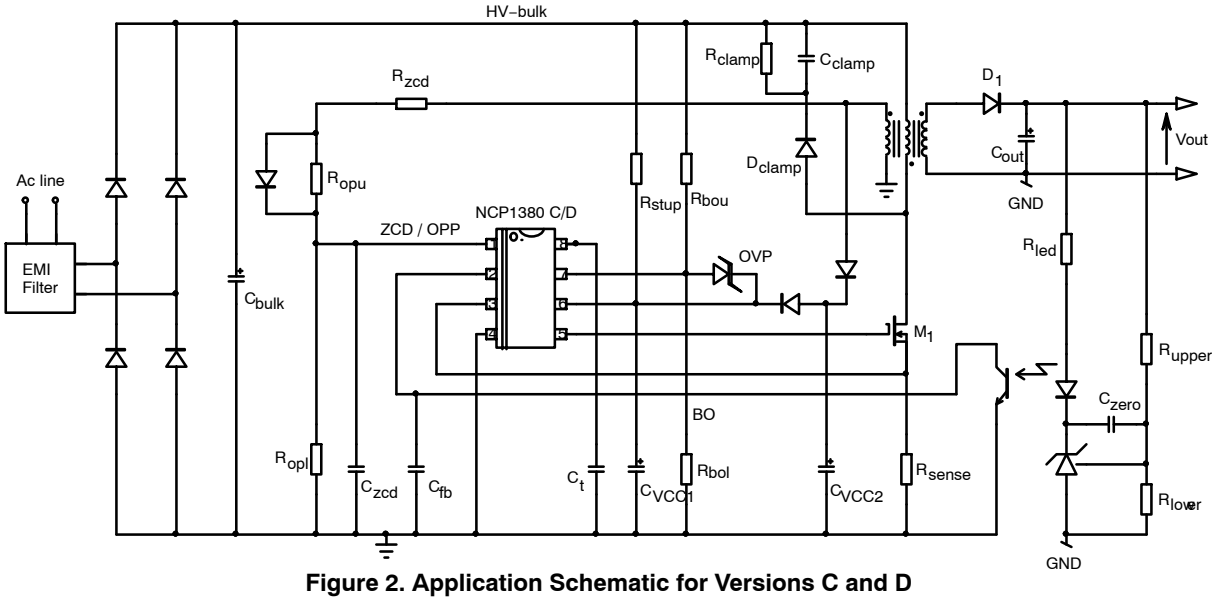

Figure 2. Application Schematic for Versions C and D

Introduction

The NCP1379 and NCP1380 implement a standard current−mode architecture operating in quasi−resonance. Due to a proprietary circuitry, the controller prevents valley−jumping instability and steadily locks out in selected valley as the power demand goes down. Once the fourth valley is reached, the controller continues to reduce the frequency further down, offering excellent efficiency over a wide operating range. Due to a fault timer combined to an OPP circuitry, the controller is able to efficiently limit the output power at high−line.

- Quasi−Resonance Current−mode operation: implementing quasi−resonance operation in peak current−mode control, the NCP1379 and NCP1380 optimize the efficiency by switching in the valley of the MOSFET drain−source voltage. Due to a proprietary circuitry, the controller locks−out in a selected valley and remains locked until the output loading significantly changes. When the load becomes lighter, the controller jumps into the next valley. It can go down to the 4th valley if necessary. Beyond this point, the controller reduces its switching frequency by freezing the peak current setpoint. During quasi−resonance operation, in case of very damped valleys, a 5.5 μs timer emulates the missing valleys.
- Frequency reduction in light−load conditions: when the 4th valley is left, the controller reduces the switching frequency which naturally improves the standby power by a reduction of all switching losses.
- Overpower protection (OPP): When the voltage on ZCD pin swings in flyback polarity, a direct image if the input voltage is applied on ZCD pin. We can thus reduce the peak current depending of V_{ZCD} during the on−time.
- Internal soft−start: a soft−start precludes the main power switch from being stressed upon start−up. Its duration is fixed and equal to 4 ms.
- Fault input (NCP1380 A and B versions): by combining a dual threshold on the Fault pin, the controller allows the direct connection of an NTC to ground plus a zener diode to a monitored voltage. In case the pin is brought below the OTP threshold by the NTC or above the OVP threshold by the zener diode, the circuit permanently latches−off and V_{CC} is clamped to 7.2 V.
- Fault input (NCP1380 C and D versions and NCP1379): the C and D versions of NCP1380 and the NCP1379 include a brown−out circuit which safely stops the controller in case the input voltage is too low. Restart occurs via a complete startup sequence (latch reset and soft−start). During normal operation, the voltage on this pin is clamped to V_{clamp} to give enough room for OVP detection. If the voltage on this pin increases above 2.5 V, the part latches−off.
- Short−circuit protection: short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (where the auxiliary winding level does not properly collapse in presence of an output short). Here, when the internal 0.8 V maximum peak current limit is activated, the timer starts counting up. If the fault disappears, the timer counts down. If the timer reaches completion while the error flag is still present, the controller stops the pulses. This protection is latched on A and C version (the user must unplug and re−plug the power supply to restart the controller) and auto−recovery on B and D versions (if the fault disappears, the SMPS automatically resumes operation). In addition, all versions feature a winding short−circuit protection, that senses the CS signal and stops the controller if V_{CS} reaches 1.5 x V_{ILIM} (after a reduced LEB of t_{BCS}). This additional comparator is enabled only during the main LEB duration t_{LEB}, for noise immunity reason.

Specifications of the Adapter

In order to illustrate this application note, a 19 V, 60 W adapter will be the design example. The specifications are detailed in Table 1.

Table 1. SPECIFICATIONS OF THE 19 V, 60 W ADAPTER

Parameter	Symbol	Value
Minimum input voltage	$V_{in(min)}$	85 Vrms
Maximum input voltage	$V_{in(max)}$	265 Vrms
Output voltage	V_{out}	19 V
Nominal output power	$P_{out(nom)}$	60 W
Switching frequency at $V_{in(min)}$, $P_{out(nom)}$	F_{sw}	45 kHz
Maximum startup time	$T_{startup}$	3 s

The experimental results of the 60 W adapter are detailed in the application note NCP1380EVB/D [1].
For details concerning the QR transformer calculation, the power supply designer can refer to the tutorial TND348/D [2].

Predicting the Switching Frequency

As the controller changes valley as the load decreases, the switching frequency of the power supply is naturally limited by the valley lockout. But equations are needed to predict the switching frequency evolution as the output power varies.

The datasheet gives the FB thresholds at which the controller changes valley, depending if the output power increases or decreases.

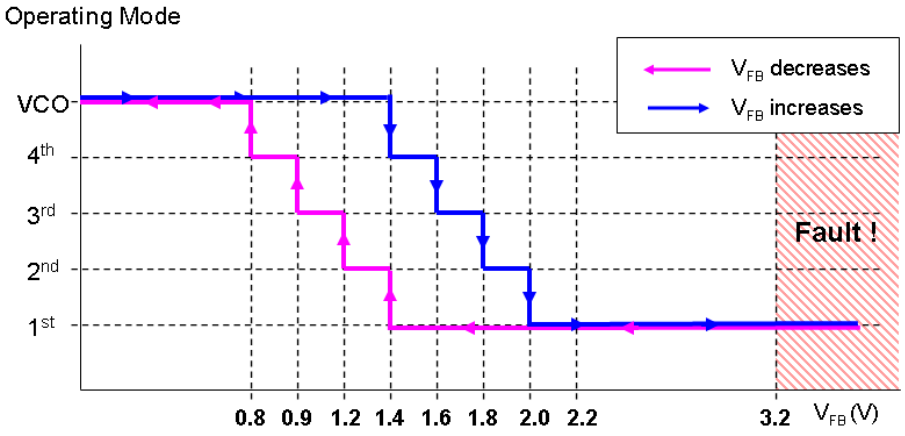

Figure 3. Operating Valley According to FB Voltage

With these thresholds, we can calculate the maximum switching frequency inside each valley depending if the output power decreases or increases:

$$F_{SW} = \frac{1}{\left(\frac{V_{FB}}{4R_{sense}} + V_{in(rms)}\sqrt{2}\frac{t_{prop}}{L_p}\right)L_p\left(\frac{1}{V_{in(rms)}\sqrt{2}} + \frac{N_{ps}}{V_{out}+V_f}\right) + (1 + 2n)\pi\sqrt{L_pC_{lump}}} \quad \text{(eq. 1)}$$

Where:

- V_{FB} is the FB threshold at which the controller changes valley
- R_{sense} is the sense resistor value
- $V_{in(rms)}$ is the rms value of the input voltage
- t_{prop} is the propagation delay
- L_p is the primary inductance
- V_{out} is the output voltage
- V_f is the forward voltage drop of the output diode

- C_{lump} regroups all capacitances surrounding the drain node (MOSFET capacitor, transformer parasitics...). As a first approximation, the MOSFET drain−source capacitance C_{OSS} can be used instead of C_{lump}.
- n is an integer representing the operating valley: n = 0 for 1st valley, n = 1 for 2nd valley, n = 2 for 3rd valley and n = 3 for the 4th valley.

The corresponding output power can be calculated using the traditional formula:

$$P_{out} = \frac{1}{2} L_p \left(\frac{V_{FB}}{4R_{sense}} + V_{in(rms)} \sqrt{2} \frac{t_{prop}}{L_p} \right)^2 F_{SW} \eta \qquad \text{(eq. 2)}$$

Using the previous equations, we can calculate the maxima of the switching frequency and the corresponding output power for our 60 W adapter.

In order to help the power supply designer, the previous equations have been entered inside a Mathcad spreadsheet that automatically predicts the evolution of the switching frequency as a function of the output power (Figure 4).

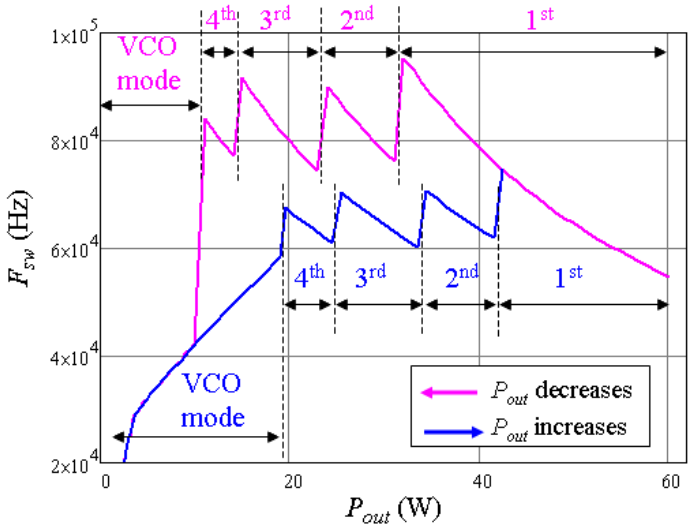

Figure 4. Switching Frequency versus Output Power at V_{in} = 90 Vrms

VCO Mode

1. **Operating Details**

At nominal power, the power supply operates in a variable frequency system where discrete frequency steps occur as the controller looks for the different valley positions.

At low output power, the controller enters a Voltage−Controlled Oscillator (VCO) mode where the switching frequency is folded back. This mode is entered when V_{FB} drops below 0.8 V. The controller remains in this mode until V_{FB} increases above 1.4 V. During the VCO operation (V_{FB} < 0.8 V), the peak current is frozen to 17.5% of its maximum value and the frequency diminishes as the output power decreases.

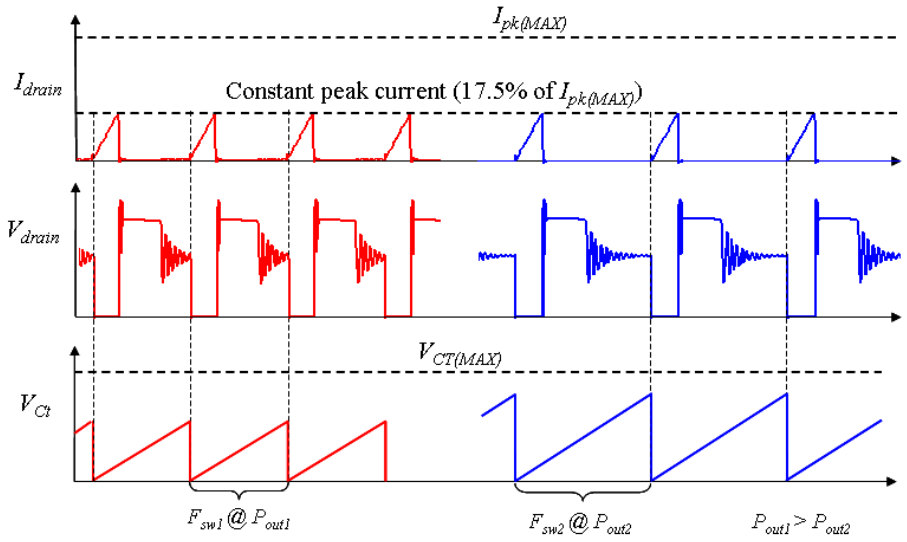

Figure 5. I_{drain}, V_{drain}, V_{Ct}, at Different Output Loads in VCO Mode

2. **Choosing the Timing Capacitor C_t**

The timing capacitor must be selected with care. Indeed, when the controller leaves the valley switching mode to enter the VCO mode, the frequency changes from a valley−position−controlled value to a switching frequency imposed by the C_t capacitor. If a too big gap exists between the switching frequency in the 4th valley and the switching frequency imposed by the C_t capacitor, the frequency jump may create instability: hesitation between 4th valley and the VCO mode takes place (Figure 6) and can create output ripple and noise.

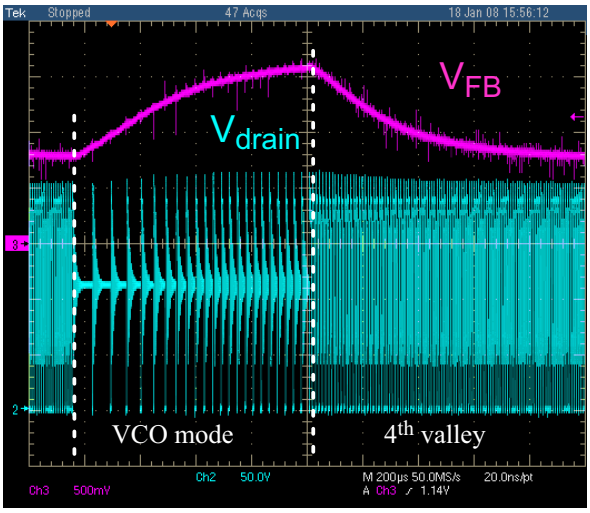

Figure 6. The Controller Hesitates Between VCO Mode and 4th Valley: C_t is Too Big!

Figure 7 shows a normal transition from 4th valley to the VCO mode. At the beginning, the output load is such that it imposes a V_{FB} near 0.8 V in 4th valley operation, with a switching period T_{sw1}. Then, if the load is slightly decreased, the FB voltage also passes below the 0.8 V threshold: the VCO mode is entered and the switching frequency decreases. (In VCO mode, the switching frequency is imposed by the FB voltage regardless of the position in the drain signal). The controller will stay in VCO mode until the FB voltage increases above 1.4 V. If we have an optimum timing capacitor value, the new steady state point is such that V_{FB} is near 1.4 V and imposes a switching period T_{sw2} larger than T_{sw1}.

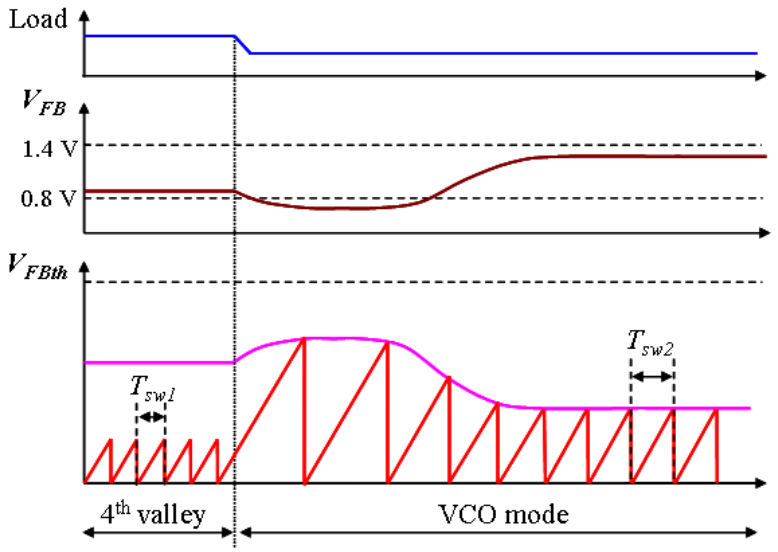

Figure 7. 4th Valley to VCO Mode Transition with an Optimum Timing Capacitor C_t

To calculate C_t, we first need to estimate the switching period at the end of the 4th valley operation, for a FB voltage near 0.8 V by using Equation 3 or by directly measuring it on our adapter:

$$T_{SW} = \left(\frac{0.8}{4R_{sense}} + V_{in(max)}\sqrt{2}\frac{t_{prop}}{L_p}\right)L_p\left(\frac{1}{V_{in(max)}\sqrt{2}} + \frac{N_{ps}}{V_{out} + V_f}\right) + 7\pi\sqrt{L_pC_{lump}} \quad \text{(eq. 3)}$$

Where:

- 0.8 is the FB voltage where the controller leaves the 4th valley and enter VCO mode.
- $V_{in(max)}$ is the maximum input voltage
- Based on lab experiments, the switching period gap between the end of 4th valley operation (T_{sw1}) and VCO mode (T_{sw2}) for a FB voltage near 1.4 V (which is the threshold for VCO mode to 4th valley transition, V_{FB} increasing) must not exceed 10 µs. Thus, for V_{FB} = 1.4 V, we will have:

$$T_{SW2} = T_{SW1} + 8\ \mu s \quad \text{(eq. 4)}$$

In VCO mode, the timing capacitor voltage V_{Ct} is dependant of the FB voltage as follows:

$$V_{Ct} = 6.5 - \frac{10}{3}V_{FB} \quad \text{(eq. 5)}$$

The Equation 5 allows calculating V_{Ct} for V_{FB} = 1.4 V:

$$V_{Ct} = 6.5 - (10/3) \times 1.4 = 1.83\ V \quad \text{(eq. 6)}$$

Thus, we can deduce the timing capacitor value knowing V_{Ct}, T_{sw2} and the charging current source I_{Ct} (20 µA typ from datasheet):

$$C_t = \frac{I_{Ct}T_{SW2}}{1.83} \quad \text{(eq. 7)}$$

Application Example: 19 V, 60 W Adapter

- $V_{in(max)}$ = 265 Vrms
- $V_{out} + V_f$ = 19 + 0.8 V
- L_p = 285 µH
- C_{lump} = 250 pF
- N_{ps} = 0.25
- R_{sense} = 0.23

First, with Equation 3, we estimate T_{sw1} which is the switching period of our power supply for an output load corresponding to a V_{FB} = 0.8 V:

$$T_{SW1} = \left(\frac{0.8}{4R_{sense}} + V_{in(max)}\sqrt{2}\frac{t_{prop}}{L_p}\right)L_p\left(\frac{1}{V_{in(max)}\sqrt{2}} + \frac{N_{ps}}{V_{out} + V_f}\right) + 7\pi\sqrt{L_pC_{lump}}$$

$$= \left(\frac{0.8}{4 \times 0.23} + 265\sqrt{2}\frac{300x10^{-9}}{285x10^{-6}}\right)285x10^{-6}\left(\frac{1}{265\sqrt{2}} + \frac{0.25}{19 + 0.8}\right) + 7\pi\sqrt{285x10^{-6} \times 250x10^{-12}} \quad \text{(eq. 8)}$$

$$= 10.7\ \mu s(93\ kHz)$$

When measured on the adapter we obtain: T_{sw1} = 11.1 μs (F_{sw1} = 90 kHz) which corresponds to an output power of 23 W. We calculate the timing capacitor value:

$$C_t = \frac{I_{Ct}(T_{SW1} + 10\mu)}{1.83} = \frac{20x10^{-6}(10.7x10^{-6} + 10x10^{-6})}{1.83} = 226\ pF \quad \text{(eq. 9)}$$

We select C_t = 200 pF.

Zero Crossing Detection

The NCP1380 combines on a single pin the inductor reset detection and the Over Power Protection (OPP). Zero crossing detection and OPP are achieved by observing the auxiliary winding voltage.

The negative part of the voltage is used for the over power protection and the positive part is used for zero crossing detection. The schematic of the zero−crossing detection bloc is shown in Figure 8.

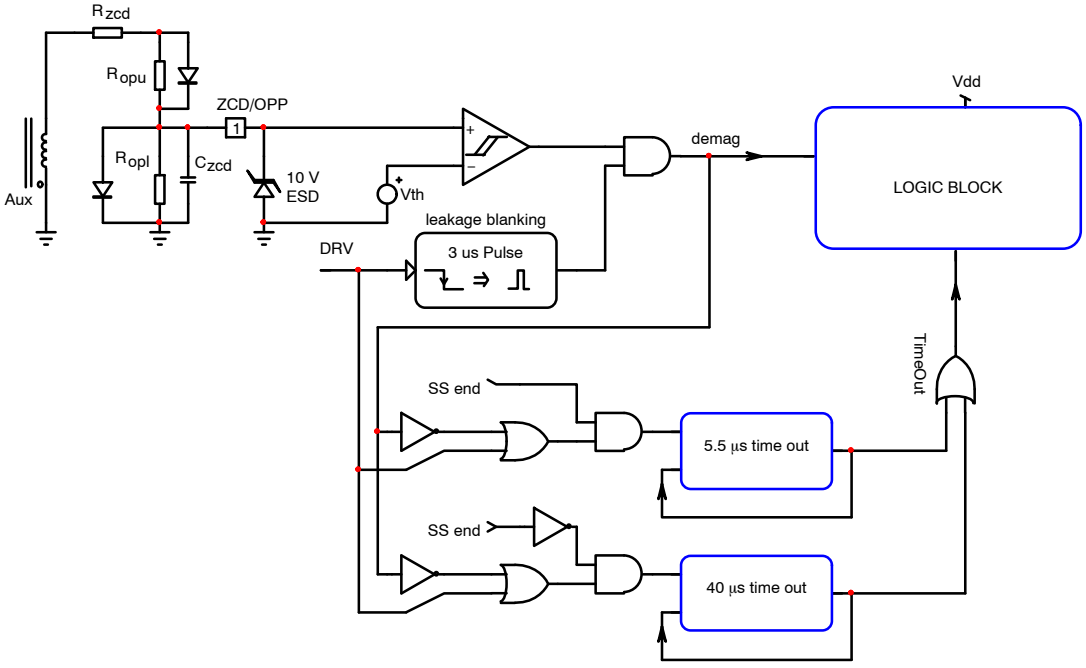

Figure 8. Zero−Crossing Detection Bloc Schematic

1. **Choosing the zero−crossing resistor (R_{zcd}) value**

In order to allow enough voltage on the ZCD pin during soft−start, the ratio between R_{zcd} and R_{opl} should be equal to 1 or lower than 1:

$$\frac{R_{zcd}}{R_{opl}} \leq 1 \quad \text{(eq. 10)}$$

Practically, we recommended a value of 1 kΩ for R_{zcd} and to keep the value of R_{opl} in the range of 1 kΩ to 3 kΩ.

2. **Time Out**

In case of extremely damped free oscillations, the ZCD comparator can be unable to detect the valleys. To avoid such situation, NCP1380 integrates a Time Out function that acts as a substitute clock for the decimal counter inside the logic bloc. The controller thus continues its normal operation. To avoid having a too big step in frequency, the time−out duration is set to 5.5 μs.

The NCP1380 also features an extended time out during the soft−start. Indeed, at startup, the output voltage reflected on the auxiliary winding is low. Because of the voltage drop introduced by the Over Power Compensation diode (Figure 9) the voltage on the ZCD pin is very low and the ZCD comparator might be unable to detect the valleys. In this condition, setting the DRV Latch with the normal 5 μs time−out leads to a continuous conduction mode operation (CCM) at the beginning of the soft−start. This CCM operation only last a few cycles until the voltage on ZCD pin becomes high enough to be detected by the ZCD comparator. To avoid this, the time−out duration is extended to 40 μs during the soft−start in order to ensure that the transformer is fully demagnetized before the MOSFET is turned−on.

Over Power Protection

1. **Operating Details**

A flyback operated in Quasi Resonance exhibits wide peak current variations in relationship to the input voltage conditions. As a result, the converter output power range widens as the input voltage increases. To cope with safety requirements, the designer needs to limit the power output capability over the input voltage range. A possible way of doing it is call Over Power Protection (OPP).

Please note that a quasi−resonant converter output power cannot be limited to a very tight range for a universal input voltage specification (85 Vrms to 265 Vrms). Indeed, the quasi−resonance mode exhibits high current slope in the transformer, causing wide peak current variation over the input voltage range compared to a Continuous Conduction Mode (CCM) design. Thus, if a very tight range for the output power capability is needed, the power supply designer should use a CCM design.

The novel technique implemented in the NCP1380 and the NCP1379 takes benefits of the auxiliary winding voltage whose negative amplitude relates to the input rail voltage. When the power MOSFET is conducting, the auxiliary winding voltage becomes the input voltage V_{in} affected by the auxiliary to primary turn ratio ($N_{p,aux} = N_{aux}/N_p$):

$$V_{aux} = -N_{p,aux}V_{in} \qquad \text{(eq. 11)}$$

By applying this voltage through a resistor divider on the ZCD pin, we have an image of the input voltage transferred to the controller via this pin. This voltage is added internally to the 0.8 V reference and affects the maximum peak current (Figure 9). As the OPP voltage is negative, an increase of input voltage implies a decrease of the maximum peak current setpoint:

$$V_{CS(max)} = 0.8 + V_{OPP} \qquad \text{(eq. 12)}$$

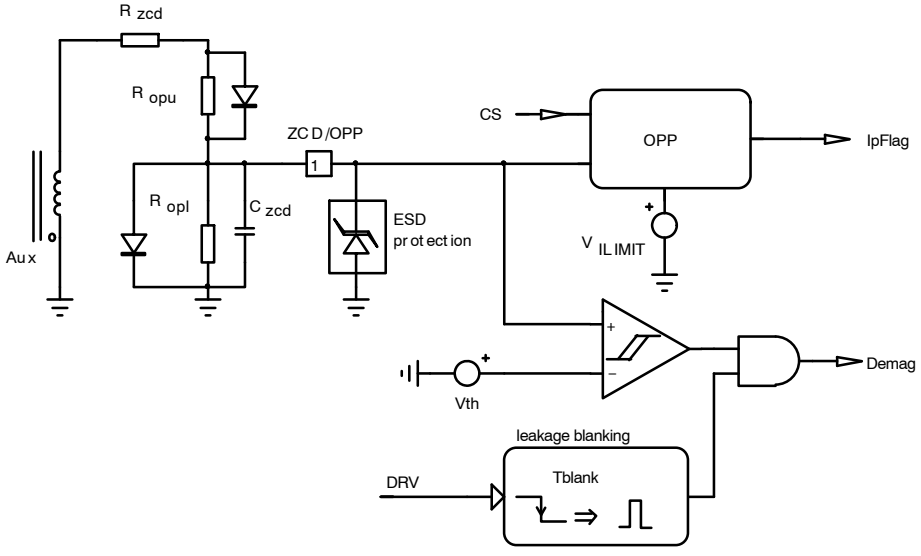

Figure 9. ZCD and OPP Circuit

The maximum OPP voltage that can be applied to ZCD pin is –300 mV, which corresponds to a peak current decrease of 37.5%. In order to avoid saturating the input transistors of the OPP comparator, the positive voltage excursion on the ZCD pin must also be limited. Thus, we recommend adding a diode between ZCD and GND to limit the positive voltage to 0.6 V. This is not mandatory, but if higher positives voltages are applied to this pin, the propagation delay of the OPP comparator will increase.

2. **Calculating the needed OPP amount for the design**

Because of the propagation delay, the maximum peak current at high line is:

$$I_{pk(high)} = \frac{0.8}{R_{sense}} + V_{in(max),dc}\frac{t_{prop}}{L_p} \qquad \text{(eq. 13)}$$

The corresponding switching period and output power are:

$$T_{SW(high)} = I_{pk(high)}L_p\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f}\right) + \pi\sqrt{L_pC_{lump}} \qquad \text{(eq. 14)}$$

$$P_{out(high)} = \frac{1}{2}L_pI_{pk(high)}{}^2\frac{1}{T_{SW(high)}}\eta \qquad \text{(eq. 15)}$$

We would like to limit the output power to $P_{out(limit)} > P_{out(nom)}$ at maximum input voltage. In order to perform over power compensation, we need to calculate the peak current $I_{pk(limit)}$ corresponding to $P_{out(limit)}$.

$$I_{pk(limit)} = \frac{L_p\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right) + \sqrt{L_p{}^2\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right)^2 + 2\frac{L_p\eta}{P_{out(limit)}}\pi\sqrt{L_pC_{lump}}}}{\frac{L_p\eta}{P_{out(limit)}}} \qquad \text{(eq. 16)}$$

The amount of OPP voltage needed is thus:

$$V_{OPP} = 0.8\left(1 - \frac{I_{pk(limit)}}{I_{pk(max)}}\right) \qquad \text{(eq. 17)}$$

As an example, in order to provide a 15% power margin to our 60 W adapter, we want to limit the output power to 70 W at high line.

Using Equations 13 to 15, we obtain:

$$I_{pk(high)} = \frac{0.8}{4R_{sense}} + V_{in(max),dc}\frac{t_{prop}}{L_p} = \frac{0.8}{4 \times 0.23} + 375\frac{600x10^{-9}}{285x10^{-6}} = 4.32\ A \qquad \text{(eq. 18)}$$

$$T_{SW(high)} = I_{pk(high)}L_p\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f}\right) + \pi\sqrt{L_pC_{lump}}$$
$$= 4.32 \times 285x10^{-6}\left(\frac{1}{375} + \frac{0.25}{19 + 0.8}\right) + \pi\sqrt{285x10^{-6} \times 250x10^{-12}} = 19.5\ \mu s \qquad \text{(eq. 19)}$$

$$P_{out(high)} = \frac{1}{2}L_pI_{pk(high)}{}^2\frac{1}{T_{SW(high)}}\eta = \frac{1}{2}285x10^{-6} \times 4.32^2\frac{1}{19.5x10^{-6}}0.85 = 116\ W \qquad \text{(eq. 20)}$$

If no over power compensation is applied, the adapter will be able to deliver 116 W at high line! In order to limit the output power to 70 W at 265 Vrms, the peak current must be reduced to:

$$I_{pk(limit)} = \frac{L_p\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right) + \sqrt{L_p{}^2\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right)^2 + 2\frac{L_p\eta}{P_{out(limit)}}\pi\sqrt{L_pC_{lump}}}}{\frac{L_p\eta}{P_{out(limit)}}} \quad \text{(eq. 21)}$$

$$= \frac{285x10^{-6}\left(\frac{1}{375} + \frac{0.25}{19+0.8}\right) + \sqrt{(285x10^{-6})^2\left(\frac{1}{375} + \frac{0.25}{19+8}\right)^2 + 2\frac{285x10^{-6}\times 0.85}{70}\pi\sqrt{285x10^{-6}\times 250x10^{-12}}}}{\frac{285x10^{-6}\times 0.85}{70}}$$

$$= 2.67\ A$$

The amount of OPP voltage that must be applied to the design is:

$$V_{OPP} = 0.8\left(1 - \frac{I_{pk(limit)}}{I_{pk(max)}}\right) = 0.8\left(1 - \frac{2.67}{4.32}\right) = 300\ mV \quad \text{(eq. 22)}$$

3. **Calculating the OPP resistors**

Looking at Figure 9, if we apply the resistor divider law on the pin 1 during the on−time, we obtain the following relationship:

$$\frac{R_{zcd} + R_{opu}}{R_{opl}} = \frac{N_{p,aux}V_{in,dc} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 23)}$$

By choosing a value for R_{opl} (for example 1 kΩ), we can easily deduce R_{opu} as we already know R_{zcd} value.
Following our example from before, we need 300 mV of OPP voltage to limit the output power to 70 W at 265 Vrms. We choose: R_{opl} = 1 kΩ

$$R_{opu} = \frac{N_{p,aux}V_{in,dc} - V_{OPP}}{V_{OPP}}R_{opl} - R_{zcd} = \frac{0.18\times 375 - (0.3)}{(0.3)}1000 - 1000 = 223\ k\Omega \quad \text{(eq. 24)}$$

Finally, we choose a 220 kΩ resistor for R_{opu}.

4. **A Non−Dissipative OPP**

The input voltage information is given by the auxiliary winding which offers lower voltage values compared to the bulk rail. In addition, in VCO mode, the switching frequency expands. Thus, the average current in the OPP bridge decreases. Let us calculate the average current circulating in the OPP bridge at light load:

$$I_{bridge(mean)} = \frac{1}{T_{SW}}\int_0^{T_{SW}}\left|\frac{V_{aux}(t)}{R_{zcd} + R_{opu} + R_{opl}}\right|dt \quad \text{(eq. 25)}$$

We obtain:

$$I_{bridge(mean)} = \frac{1}{R_{zcd} + R_{opu} + R_{opl}}\frac{t_{on}}{T_{SW}}N_{p,aux}V_{in}\sqrt{2} + \frac{1}{R_{opu} + R_{opl}}\frac{t_{off}}{T_{SW}}\left(V_{CC} + V_f\right) \quad \text{(eq. 26)}$$

On our 60 W adapter, for an output power of 4 W, we measured:

- t_{on} = 1.2 μs
- t_{off} = 3.6 μs
- T_{sw} = 40 μs
- $V_{CC} + V_f$ = 12 V

We can calculate the OPP bridge current at highest input voltage (265 Vrms):

$$I_{bridge(mean)} = \frac{1}{R_{zcd} + R_{opu} + R_{opl}}\frac{t_{on}}{T_{SW}}N_{p,aux}V_{in}\sqrt{2} + \frac{1}{R_{opu} + R_{opl}}\frac{T_{off}}{T_{SW}}\left(V_{CC} + V_f\right)$$

$$= \frac{1}{220k + 1k + 1k}\frac{1.2\mu}{40\mu}0.18\times 265\sqrt{2} + \frac{1}{220k + 1k}\frac{3.6\mu}{40\mu}12 = 14\ \mu A \quad \text{(eq. 27)}$$

As the bridge current is very low, the power dissipated by the OPP bridge can be neglected.

Startup Network for NCP1380

The NCP1379 has a low $V_{CC(on)}$ threshold (around 12 V), allowing to use an auxiliary power supply to bias the controller. Also, the NCP1379 will consume much current during the startup phase (1.2 mA), thus if the power designer wants to use startup resistors instead of an auxiliary power supply, the power dissipated in the startup resistors will be high.

On the contrary, the NCP1380 has an higher $V_{CC(on)}$ threshold but consumes a very low current during the startup (10 μA typ, 20 μA max). Thus, high values of startup resistors can be used leading to lower power dissipation in the startup network.

The startup resistor $R_{startup}$ can either be connected to the bulk rail or to half−wave (Figure 10). Connecting the startup resistor to the half−wave allows decreasing the power dissipated in the startup resistor.

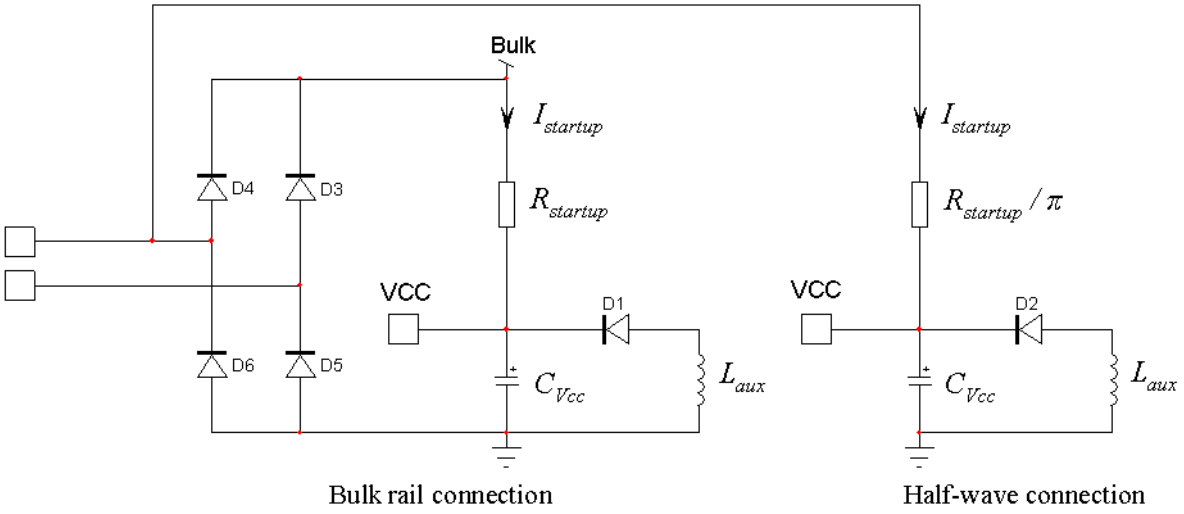

Figure 10. The Startup Resistor can be Connected to the Bulk Rail or to the Half Wave

1. **Calculating the Startup Capacitor**

The startup capacitor is calculated to allow the power supply to close the loop before V_{CC} falls below $V_{CC(off)}$. Thus, C_{Vcc} must be able to supply the controller alone during a limited time t_{reg} (Figure 11).

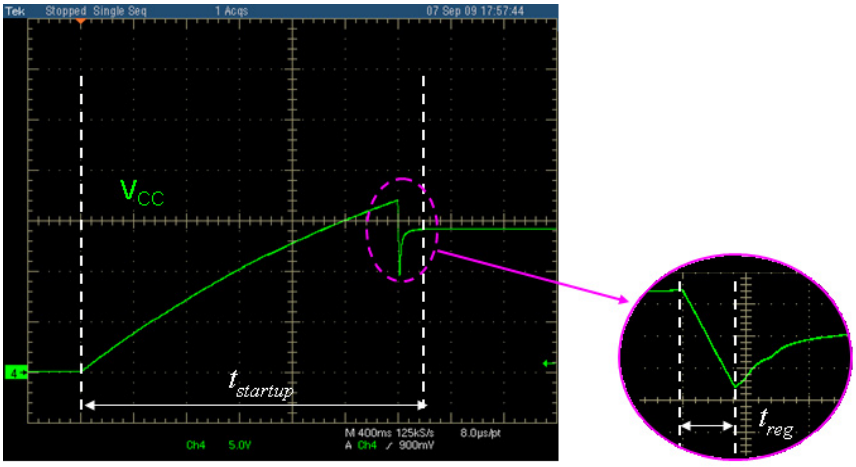

Figure 11. V_{CC} Waveform During Startup

The startup capacitor value can be calculated as follows:

$$C_{VCC} = \frac{\left(I_{CC3A} + Q_g F_{SW}\right) t_{reg}}{V_{CC(on)} - V_{CC(off)}} \qquad \text{(eq. 28)}$$

The current needed to charge C_{Vcc} alone during the startup is:

$$I_{CVCC} = \frac{V_{CC(on)}C_{VCC}}{t_{startup}} \quad \text{(eq. 29)}$$

Design Example:
For our 19 V, 60 W adapter, we chose a 9 A, 600 V MOSFET (IPA60R385 from Infineon).
The total gate charge is: Q_g = 17 nC
The switching frequency at low line, maximum output load is: F_{sw} = 45 kHz
The total startup time of the adapter must be below 3 s. We will consider a startup time $t_{startup}$ of 2.8 s.
The value of t_{reg} can be estimated around 10 ms.

From the datasheet, we can extract the values of the following parameters:
I_{CC3A} = 2.4 mA
$V_{CC(on)}$ = 17 V
$V_{CC(off)}$ = 9 V
We can deduce:

$$C_{VCC} = \frac{(I_{CC3A} + Q_g F_{SW})t_{reg}}{V_{CC(on)} - V_{CC(off)}} = \frac{(2.4m + 17n \times 45000) \times 10m}{17 - 9} = 3.9\ \mu F \quad \text{(eq. 30)}$$

We choose a 4.7 μF capacitor for C_{Vcc}.
The current needed to charge C_{Vcc} is:

$$I_{CVCC} = \frac{V_{CC(on)}C_{VCC}}{t_{startup}} = \frac{17 \times 4.7\mu}{2.8} = 28.5\ \mu A \quad \text{(eq. 31)}$$

2. **Startup Resistor Calculation**

***Bulk connection**
If the resistor is connected to the bulk rail, the following formula can be use to calculate its value:

$$R_{startup} = \frac{V_{in(min)}\sqrt{2}}{I_{CVCC} + I_{CC(start)}} \quad \text{(eq. 32)}$$

Where:

- I_{Cvcc} is the current needed to charge the V_{CC} pin capacitor
- $I_{CC(start)}$ is the current consumed by the controller during startup
- $V_{in(min)}$ is the minimum input voltage

The power dissipated by the startup resistor connected to the bulk rail is:

***Half−wave connection**
If the resistor is connected to the half−wave:

$$R_{startup1/2} = \frac{\frac{V_{in(min)}\sqrt{2}}{\pi}}{I_{CVCC} + I_{CC(start)}} = \frac{R_{startup}}{\pi} \quad \text{(eq. 33)}$$

The power dissipated by the startup resistor connected to the half−wave is thus:

$$P_{startup1/2} = \frac{\left(\frac{V_{in(max)}\sqrt{2}}{\pi} - V_{CC}\right)^2}{R_{startup1/2}} \quad \text{(eq. 34)}$$

Design Example:
From the datasheet, the maximum value of $I_{CC(start)}$ is 20 μA. We will consider a typical value of 15 μA for this parameter. In standby, the supply voltage of the controller decreases to 11 V.
We deduce:

$$R_{startup} = \frac{V_{in(min)}\sqrt{2}}{I_{CVCC} + I_{CC(start)}} = \frac{85\sqrt{2}}{28.5\mu + 10\mu} \approx 3.2\ M\Omega \quad \text{(eq. 35)}$$

$$R_{startup1/2} = \frac{\frac{V_{in(min)}\sqrt{2}}{\pi}}{I_{CVCC} + I_{CC(start)}} = \frac{\frac{85\sqrt{2}}{\pi}}{28.5\mu + 10\mu} \approx 1\ M\Omega \quad \text{(eq. 36)}$$

The power dissipated for each resistor is:

$$P_{startup} = \frac{\left(V_{in(max)}\sqrt{2} - V_{CC}\right)^2}{R_{startup}} = \frac{\left(265\sqrt{2} - 11\right)^2}{3.2x10^6} = 44\ mW \quad \text{(eq. 37)}$$

$$P_{startup1/2} = \frac{\left(\frac{V_{in(max)}\sqrt{2}}{\pi} - V_{CC}\right)^2}{R_{startup1/2}} = \frac{\left(\frac{265\sqrt{2}}{\pi} - 11\right)^2}{1x10^6} = 14\ mW \quad \text{(eq. 38)}$$

Connecting the startup resistor to the half−wave allows saving 30 mW!

Fault Pin

The Fault pin combines different safety features in order to provide compact design of power supply.

The safeties provided vary according to the version of the NCP1380 or NCP1379. Table 2 summarizes the possible combinations:

Table 2. NCP1379 AND NCP1380 FAULT PIN OPTIONS

	Over Voltage Protection	Over Temperature Protection	Brown−Out
NCP1379	✓		✓
NCP1380 A	✓	✓	
NCP1380 B	✓	✓	
NCP1380 C	✓		✓
NCP1380 D	✓		✓

1. **Over Temperature Protection**

The adapter operating in a confined area, e.g. the plastic case protecting the converter, it is important to look after the internal ambient temperature. If this temperature would increase beyond a certain point, catastrophic failures could occur through semiconductors thermal runaway or transformer saturation. To prevent this from happening, the versions A and B of the NCP1380 embed an Over Temperature Protection (OTP) circuitry which can be combined with an Over Voltage Protection appearing in Figure 12.

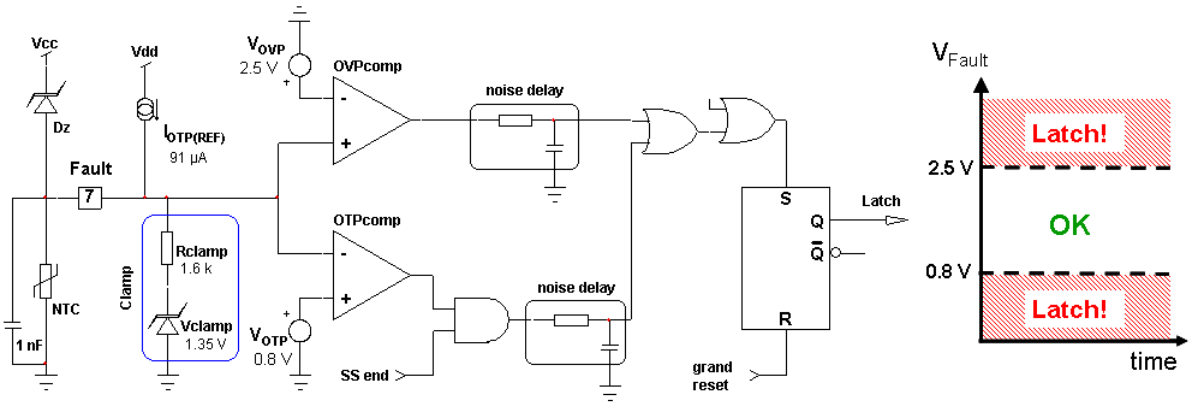

Figure 12. OTP/OVP Combination in NCP1380 A and B Versions

The $I_{OTP(REF)}$ current (91 µA typ.) biases the Negative Temperature Coefficient sensor (NTC), naturally imposing a dc voltage on the OTP pin. When the temperature increases, the NTC's resistance reduces bringing the pin 7 voltage down until it reaches a typical value of 0.8 V: the comparator trips and latches−off the controller. During the latch−off phase, the V_{CC} is pulled down to 7.2 V by an internal clamp circuit.

The controller reset occurs when the current circulating in the V_{CC} pin drop below 30 µA or when the V_{CC} is cycled from on to off.

During start−up and soft−start, the output of the OTP comparator is masked to allow the voltage on pin OTP to grow if a filtering capacitor is installed across the NTC.

The filtering capacitor value should be 1 nF.

In the NCP1380, the OTP trip point corresponds to a resistance of:

$$R_{NTC} = \frac{V_{OTP}}{I_{OTP(REF)}} = \frac{0.8}{91\mu} = 8.79\ k\Omega \qquad \text{(eq. 39)}$$

2. **Brown−Out**

The NCP1379, the C and D versions of NCP1380 feature a Brown−Out (BO) circuit which protects the power supply against low input voltage conditions (Figure 13).

The Brown−Out function is combined with an Over voltage Protection on pin 7. This pin permanently monitors a fraction of the bulk voltage through a voltage divider. When this image of bulk voltage is below the BO threshold, the controller stops switching. When the bulk voltage comes back within safe limits, the circuit goes through a new startup sequence including soft−start and re−starts switching. The hysteresis on brown−out pin is implemented with a high side current source sinking 10 µA when the brown−out comparator is high ($V_{bulk} > V_{bulk(on)}$).

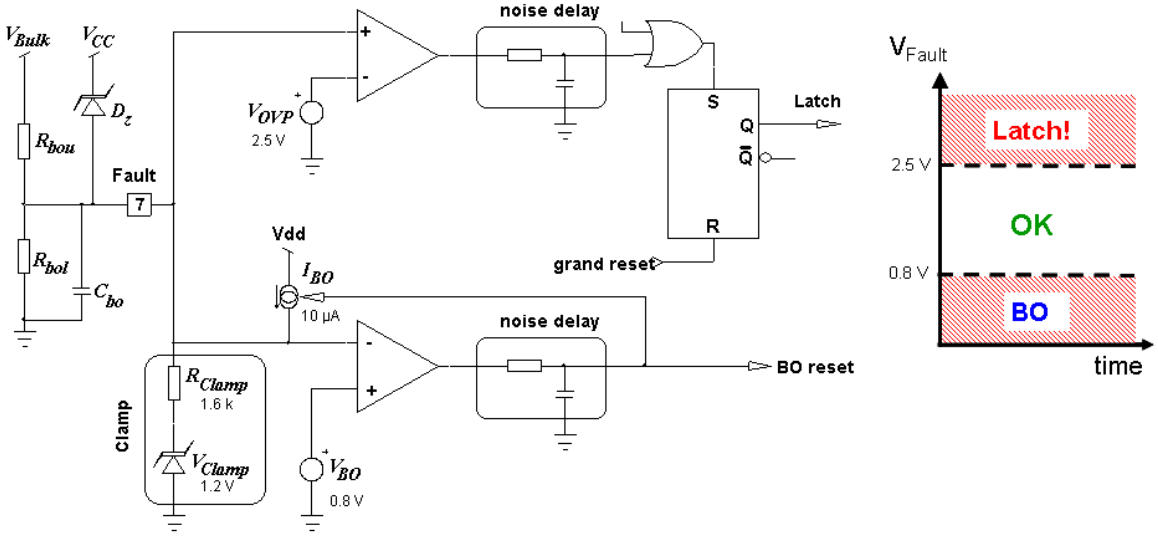

Figure 13. BO / OVP Combination in NCP1379, NCP1380 C and D Versions

Calculating the BO Resistors

The following equations show how to calculate the brownout resistors.

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulk(on)}$) and the bulk voltage for shutdown ($V_{bulk(off)}$). Then use the following equation to calculate R_{bou} and R_{bol}.

$$R_{bol} = \frac{V_{BO}\left(V_{bulk(on)} - V_{bulk(off)}\right)}{I_{BO}\left(V_{bulk(on)} - V_{BO}\right)} \quad \text{(eq. 40)}$$

$$R_{bou} = \frac{R_{bol}\left(V_{bulk(on)} - V_{BO}\right)}{V_{BO}} \quad \text{(eq. 41)}$$

Design example

- V_{BO} = 0.8 V
- I_{BO} = 10 μA
- $V_{bulk(on)}$ = 110 V
- $V_{bulk(off)}$ = 50 V

$$R_{bol} = \frac{V_{BO}\left(V_{bulk(on)} - V_{bulk(off)}\right)}{I_{BO}\left(V_{bulk(on)} - V_{BO}\right)} = \frac{0.8(110 - 50)}{10x10^{-6}(110 - 0.8)} = 43.9\ k\Omega \quad \text{(eq. 42)}$$

$$R_{bou} = \frac{R_{bol}\left(V_{bulk(on)} - V_{BO}\right)}{V_{BO}} = \frac{43.9x10^{3}(110 - 0.8)}{0.8} = 6.0\ M\Omega \quad \text{(eq. 43)}$$

3. **Over Voltage Protection**

The NCP1379 and the NCP1380 features a protection against an over voltage condition, e.g in case of the optocoupler destruction.

This over voltage protection is combined either with an OTP or a BO protection, as shown previously on Figures 12 and 13. Only a zener diode needs to be added between the V_{CC} rail and the Fault pin in order to detect an over voltage condition. In case of over voltage, the zener diode starts to conduct and inject current inside the internal clamp resistor R_{clamp} thus causing the pin 7 voltage to increase. When this voltage reaches the OVP threshold (2.5 V typ), the controller is latched−off.

The amount of current that must be injected inside the controller by the zener diode depends on the circuit version and can be calculated as follows:

$$I_{Fault} = \frac{V_{OVP} - V_{Clamp}}{R_{Clamp}} \quad \text{(eq. 44)}$$

Thus, for the NCP1379 and the NCP1380 C&D, the amount of current needed is:

$$I_{Fault} = \frac{V_{OVP} - V_{Clamp}}{R_{Clamp}} = \frac{2.5 - 1.2}{1.6x10^{3}} = 812.5\ \mu A \quad \text{(eq. 45)}$$

For the versions A and B of the NCP1380, the amount of current to be injected in the pin Fault is:

$$I_{Fault} = \frac{V_{OVP} - V_{Clamp}}{R_{Clamp}} = \frac{2.5 - 1.35}{1.6x10^{3}} = 719\ \mu A \quad \text{(eq. 46)}$$

Note: In the NCP1379, the internal latch is reset either by a BO condition or when V_{CC} falls below $V_{CC(reset)}$.

Conclusion

This application note has described the equations needed to design a QR adapter driven by the NCP1380. These equations can be applied to the NCP1379.

All the equations presented have been implemented inside a Mathcad spreadsheet that can be downloaded from our website: http://www.onsemi.com/

References

1. Stéphanie Conseil, “Performances of a 60 W Quasi−resonant adapter driven by the NCP1380”, Application Note NCP1380EVB/D.
2. Stéphanie Conseil, “QR − Analysis and Design of Quasi−Resonant Converters”, Tutorial TND348/D.

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